Low Power, Rail-to-Rail Output, Video Op Amps with Ultralow Power

ADA4853-1/ADA4853-2/ADA4853-3

FEATURES

Ultralow power-down current: 0.1 μA
Low quiescent current: 1.4 mA/amplifier
Ideal for standard definition video
High speed
- **100 MHz, −3 dB bandwidth**
- **120 V/μs slew rate**

0.5 dB flatness: 22 MHz
Differential gain: 0.20%
Differential phase: 0.10°
Single-supply operation
Rail-to-rail output
- **Output swings to within 200 mV of either rail**

Low voltage offset: 1 mV
Wide supply range: 2.65 V to 5 V

APPLICATIONS

Portable multimedia players
Video cameras
Digital still cameras
Consumer video
Clock buffer

PIN CONFIGURATIONS

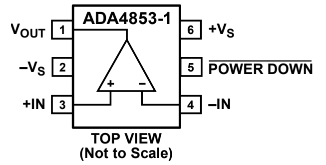


Figure 1. 6-Lead SC70

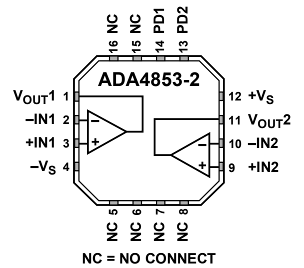


Figure 2. 16-Lead LFCSP_VQ

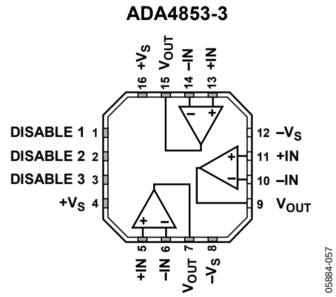


Figure 3. 16-Lead LFCSP_VQ

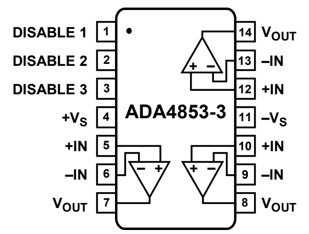


Figure 4. 14-Lead TSSOP

GENERAL DESCRIPTION

The ADA4853-1/ADA4853-2/ADA4853-3 are low power, low cost, high speed, rail-to-rail output op amps with ultralow power disables that are ideal for portable consumer electronics. Despite their low price, the ADA4853-1/ADA4853-2/ADA4853-3 provide excellent overall performance and versatility. The 100 MHz, −3 dB bandwidth, and 120 V/μs slew rate make these amplifiers well-suited for many general-purpose, high speed applications.

The ADA4853-1/ADA4853-2/ADA4853-3 voltage feedback op amps are designed to operate at supply voltages as low as 2.65 V and up to 5 V using only 1.4 mA of supply current per amplifier. To further reduce power consumption, the amplifiers are equipped with a power-down mode that lowers the supply current to less than 1.5 μA maximum, making them ideal in battery-powered applications.

The ADA4853-1/ADA4853-2/ADA4853-3 provide users with a true single-supply capability, allowing input signals to extend 200 mV below the negative rail and to within 1.2 V of the positive rail. On the output, the amplifiers can swing within 200 mV of either supply rail.

With their combination of low price, excellent differential gain (0.2%), differential phase (0.10°), and 0.5 dB flatness out to 22 MHz, these amplifiers are ideal for video applications.

The ADA4853-1 is available in a 6-lead SC70, the ADA4853-2 is available in a 16-lead LFCSP_VQ, and the ADA4853-3 is available in both a 16-lead LFCSP_VQ and a 14-lead TSSOP. The ADA4853-1 temperature range is −40°C to +85°C, while the ADA4853-2/ADA4853-3 temperature range is −40°C to +105°C.

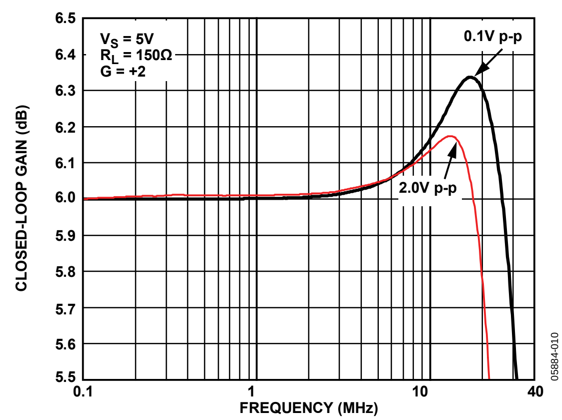


Figure 5. 0.5 dB Flatness Frequency Response

Rev. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

10/07—Rev. B to Rev. C

Changes to Applications Section ... 1
Changes to Ordering Guide ... 16

10/06—Rev. A to7 Rev. B

Added ADA4853-3 ... Universal
Added 16-Lead LFCSP_VQ ... Universal
Added 14-Lead TSSOP ... Universal
Changes to Features ... 1
Changes to DC Performance, Input Characteristics, and Power Supply Sections ... 3
Changes to DC Performance, Input Characteristics, and Power Supply Sections ... 4
Changes to Figure 20 ... 8
Changes to Figure 49 ... 13
Updated Outline Dimensions ... 16
Changes to Ordering Guide ... 16

7/06—Rev. 0 to Rev. A

Added ADA4853-2 ... Universal
Changes to Features and General Description ... 1
Changes to Table 1 ... 3
Changes to Table 2 ... 4
Changes to Table 3 ... 5
Changes to Figure 7 ... 6
Changes to Figure 11 Caption, Figure 12, Figure 13, and Figure 16 ... 7
Changes to Figure 17 and Figure 19 ... 8
Inserted Figure 21; Renumbered Sequentially ... 8
Inserted Figure 25; Renumbered Sequentially ... 9
Changes to Figure 28 ... 9
Changes to Figure 31 through Figure 35 ... 10
Changes to Figure 37, Figure 39 through Figure 42 ... 11
Inserted Figure 43 and Figure 46 ... 12
Inserted Figure 47 ... 13
Changes to Circuit Description Section ... 13
Changes to Headroom Considerations Section ... 13
Changes to Figure 48 ... 14
Updated Outline Dimensions ... 15
Changes to Ordering Guide ... 15

1/06—Revision 0: Initial Version

SPECIFICATIONS

SPECIFICATIONS WITH 3 V SUPPLY

T_A = 25°C, R_F = 1 kΩ, R_G = 1 kΩ for G = +2, R_L = 150 Ω, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.1 V p-p		90		MHz
	G = +2, V_O = 2 V p-p		32		MHz
Bandwidth for 0.5 dB Flatness	G = +2, V_O = 2 V p-p, R_L = 150 Ω		22		MHz
Settling Time to 0.1%	V_O = 2 V step		45		ns
Slew Rate	G = +2, V_O = 2 V step	88	100		V/μs
NOISE/DISTORTION PERFORMANCE					
Differential Gain	R_L = 150 Ω		0.20		%
Differential Phase	R_L = 150 Ω		0.10		Degrees
Input Voltage Noise	f = 100 kHz		22		nV/√Hz
Input Current Noise	f = 100 kHz		2.2		pA/√Hz
Crosstalk	G = +2, V_O = 2 V p-p, R_L = 150 Ω, f = 5 MHz		−66		dB
DC PERFORMANCE					
Input Offset Voltage			1	4	mV
Input Offset Voltage Drift			1.6		μV/°C
Input Bias Current			1.0	1.7	μA
Input Bias Current Drift			4		nA/°C
Input Bias Offset Current			50		nA
Open-Loop Gain	V_O = 0.5 V to 2.5 V	72	80		dB
INPUT CHARACTERISTICS					
Input Resistance	Differential/common mode		0.5/20		MΩ
Input Capacitance			0.6		pF
Input Common-Mode Voltage Range			−0.2 to +V_{CC} − 1.2		V
Input Overdrive Recovery Time (Rise/Fall)	V_{IN} = −0.5 V to +3.5 V, G = +1		40		ns
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1 V	−69	−85		dB
POWER-DOWN					
Power-Down Input Voltage	Power-down		1.2		V
Turn-Off Time			1.4		μs
Turn-On Time			120		ns
Power-Down Bias Current					
Enabled	Power-down = 3.0 V		25	30	μA
Power-Down	Power-down = 0 V		0.01		μA
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = −0.25 V to +1.75 V, G = +2		70		ns
Output Voltage Swing	R_L = 150 Ω	0.3 to 2.7	0.15 to 2.88		V
Short-Circuit Current	Sinking/sourcing		150/120		mA
POWER SUPPLY					
Operating Range		2.65		5	V
Quiescent Current/Amplifier			1.3	1.6	mA
Quiescent Current (Power-Down)/Amplifier	Power-down = low		0.1	1.5	μA
Positive Power Supply Rejection	+V_S = +1.5 V to +2.5 V, −V_S = −1.5 V	−76	−86		dB
Negative Power Supply Rejection	−V_S = −1.5 V to −2.5 V, +V_S = +1.5 V	−77	−88		dB

SPECIFICATIONS WITH 5 V SUPPLY

T_A = 25°C, R_F = 1 kΩ, R_G = 1 kΩ for G = +2, R_L = 150 Ω, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.1 V p-p		100		MHz
	G = +2, V_O = 2 V p-p		35		MHz
Bandwidth for 0.5 dB Flatness	G = +2, V_O = 2 V p-p		22		MHz
Settling Time to 0.1%	V_O = 2 V step		54		ns
Slew Rate	G = +2, V_O = 2 V step	93	120		V/μs
NOISE/DISTORTION PERFORMANCE					
Differential Gain	R_L = 150 Ω		0.22		%
Differential Phase	R_L = 150 Ω		0.10		Degrees
Input Voltage Noise	f = 100 kHz		22		nV/√Hz
Input Current Noise	f = 100 kHz		2.2		pA/√Hz
Crosstalk	G = +2, V_O = 2 V p-p, R_L = 150 Ω, f = 5 MHz		−66		dB
DC PERFORMANCE					
Input Offset Voltage			1	4.1	mV
Input Offset Voltage Drift			1.6		μV/°C
Input Bias Current			1.0	1.7	μA
Input Bias Current Drift			4		nA/°C
Input Bias Offset Current			60		nA
Open-Loop Gain	V_O = 0.5 V to 4.5 V	72	80		dB
INPUT CHARACTERISTICS					
Input Resistance	Differential/common mode		0.5/20		MΩ
Input Capacitance			0.6		pF
Input Common-Mode Voltage Range			−0.2 to +V_{CC} − 1.2		V
Input Overdrive Recovery Time (Rise/Fall)	V_{IN} = −0.5 V to +5.5 V, G = +1		40		ns
Common-Mode Rejection Ratio	V_{CM} = 0 V to 3 V	−71	−88		dB
POWER-DOWN					
Power-Down Input Voltage	Power-down		1.2		V
Turn-Off Time			1.5		μs
Turn-On Time			120		ns
Power-Down Bias Current					
Enabled	Power-down = 5 V		40	50	μA
Power-Down	Power-down = 0 V		0.01		μA
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = −0.25 V to +2.75 V, G = +2		55		ns
Output Voltage Swing	R_L = 75 Ω	0.55 to 4.5	0.1 to 4.8		V
Short-Circuit Current	Sinking/sourcing		160/120		mA
POWER SUPPLY					
Operating Range		2.65		5	V
Quiescent Current/Amplifier			1.4	1.8	mA
Quiescent Current (Power-Down)/Amplifier	Power-down = low		0.1	1.5	μA
Positive Power Supply Rejection	+V_S = +2.5 V to +3.5 V, −V_S = −2.5 V	−75	−80		dB
Negative Power Supply Rejection	−V_S = −2.5 V to −3.5 V, +V_S = +2.5 V	−75	−80		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	5.5 V
Power Dissipation	See Figure 6
Common-Mode Input Voltage	$-V_S - 0.2$ V to $+V_S - 1.2$ V
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	
6-Lead SC70	−40°C to +85°C
16-Lead LFCSP_VQ	−40°C to +105°C
14-Lead TSSOP	−40°C to +105°C
Lead Temperature	JEDEC J-STD-20
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in the circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	Unit
6-Lead SC70	430	°C/W
16-Lead LFCSP_VQ	63	°C/W
14-Lead TSSOP	120	°C/W

Maximum Power Dissipation

The maximum safe power dissipation for the ADA4853-1/ ADA4853-2/ADA4853-3 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a junction temperature of 150°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) for a sine wave and a resistor load is the total power consumed from the supply minus the load power.

$$P_D = \textit{Total Power Consumed} - \textit{Load Power}$$

$$P_D = \left(V_{SUPPLY\ VOLTAGE} \times I_{SUPPLY\ CURRENT}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads and through holes under the device reduces θ_{JA}.

Figure 6 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 6-lead SC70 (430°C/W), the 14-lead TSSOP (120°C/W), and the 16-lead LFCSP_VQ (63°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

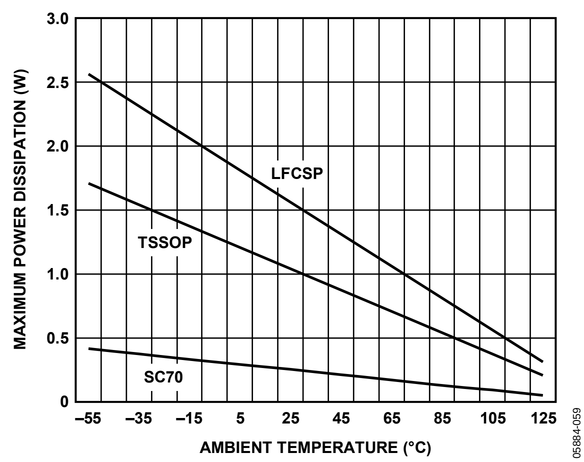
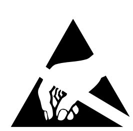


Figure 6. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

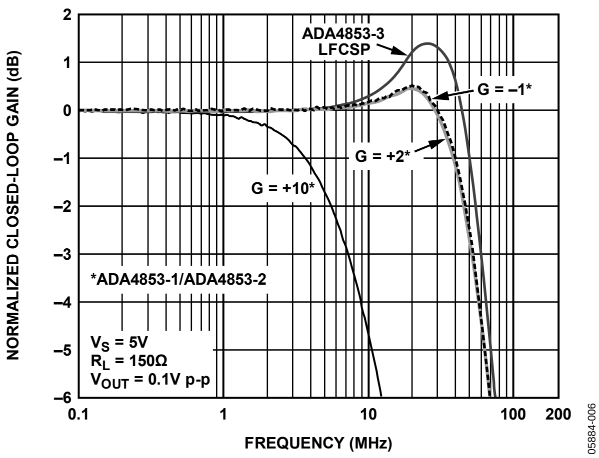


Figure 7. Small Signal Frequency Response for Various Gains

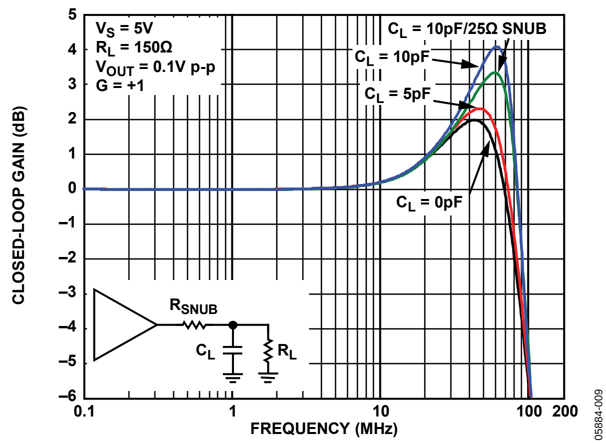


Figure 10. Small Signal Frequency Response for Various Capacitive Loads

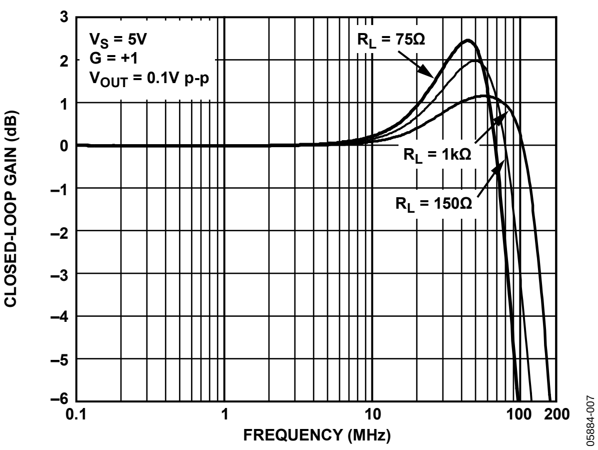


Figure 8. Small Signal Frequency Response for Various Loads

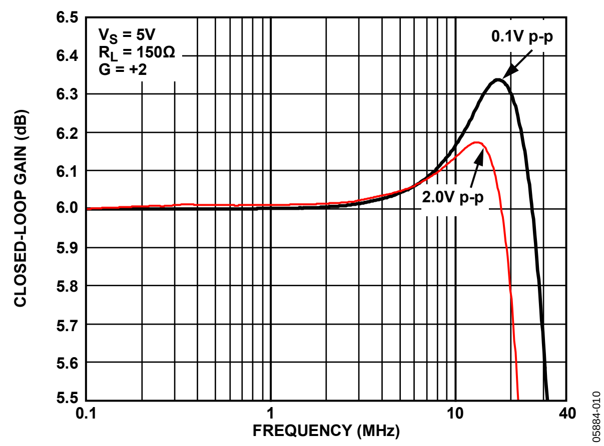


Figure 11. 0.5 dB Flatness Response for Various Output Voltages

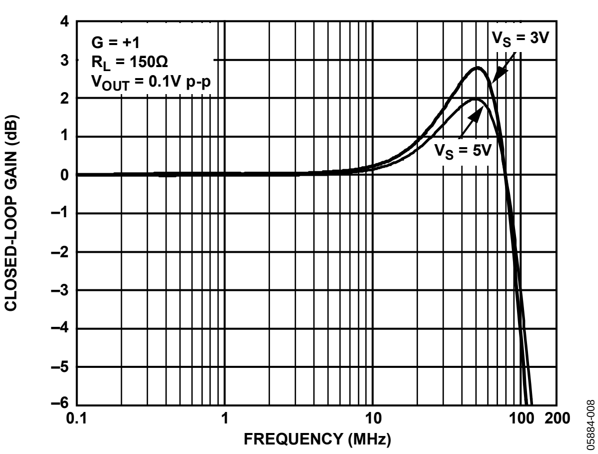


Figure 9. Small Signal Frequency Response for Various Supplies

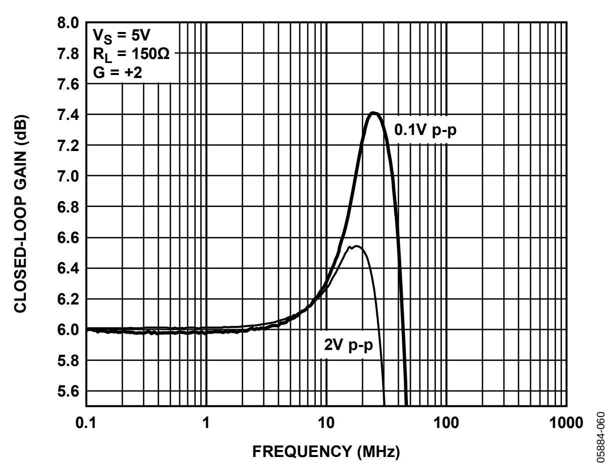


Figure 12. ADA4853-3 LFCSP_VQ Flatness Response for Various Output Voltages

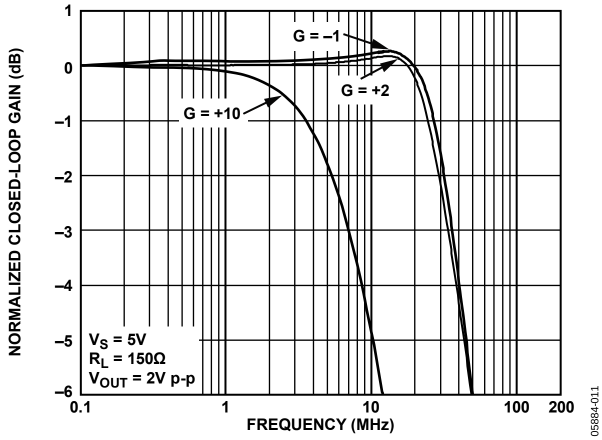


Figure 13. Large Signal Frequency Response for Various Gains

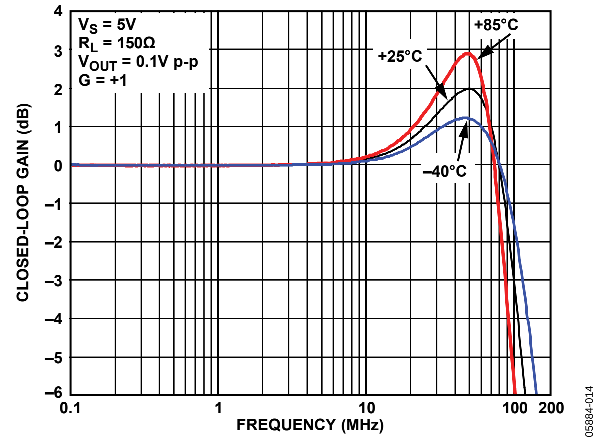


Figure 16. Small Signal Frequency Response for Various Temperatures

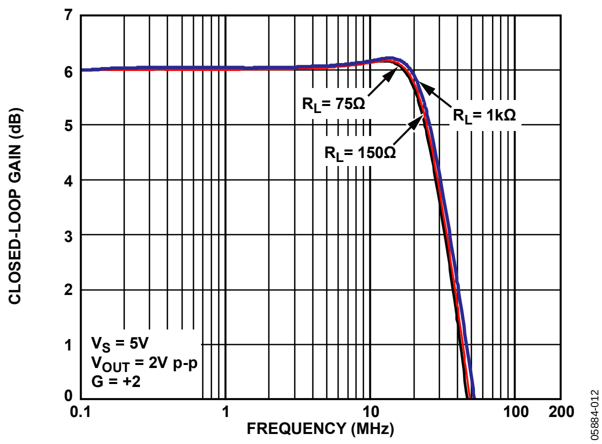


Figure 14. Large Signal Frequency Response for Various Loads

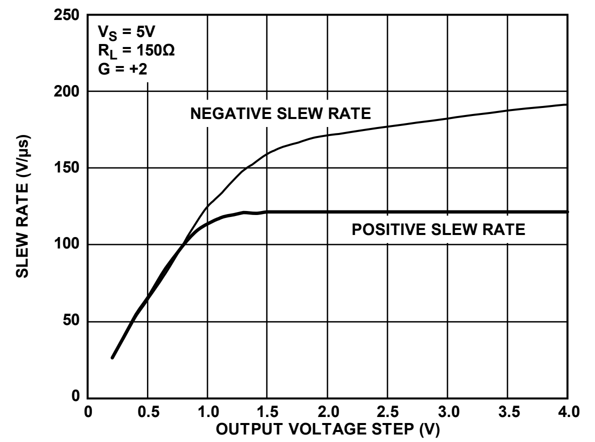


Figure 17. Slew Rate vs. Output Voltage

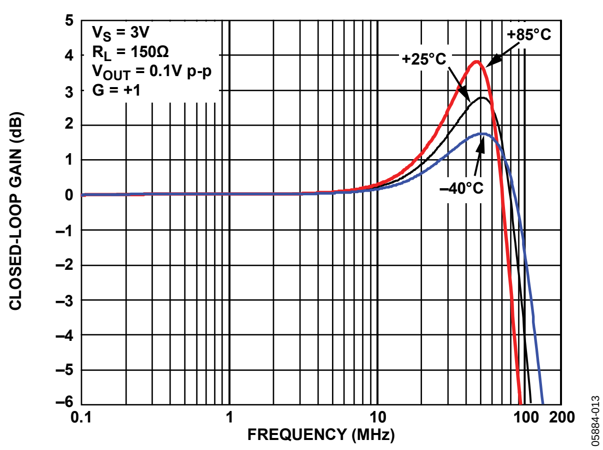


Figure 15. Small Signal Frequency Response for Various Temperatures

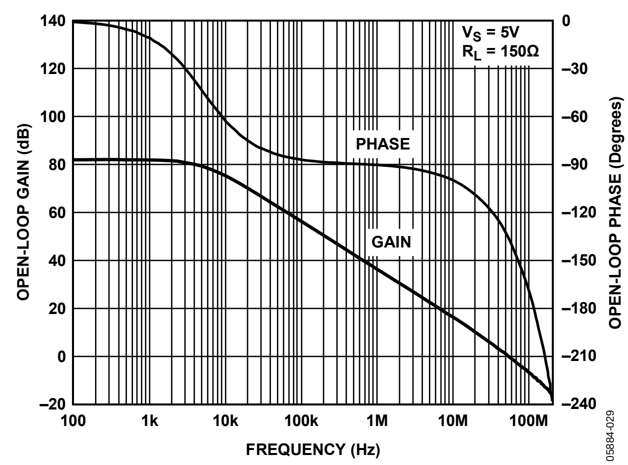


Figure 18. Open-Loop Gain and Phase vs. Frequency

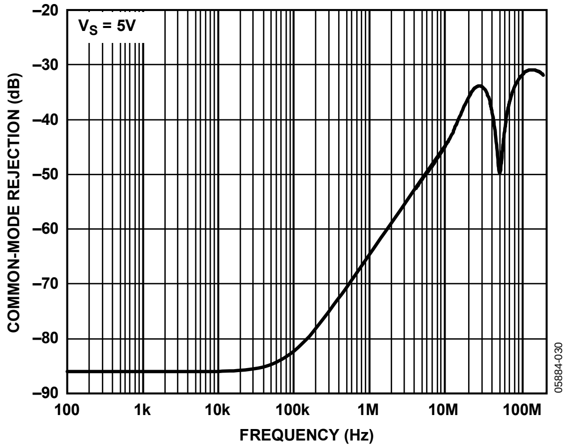


Figure 19. Common-Mode Rejection vs. Frequency

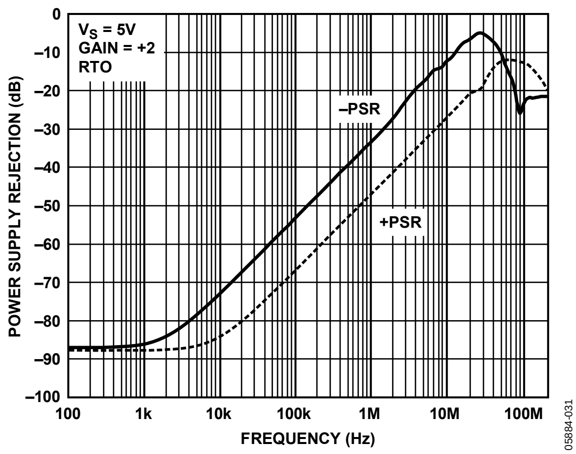


Figure 20. Power Supply Rejection vs. Frequency

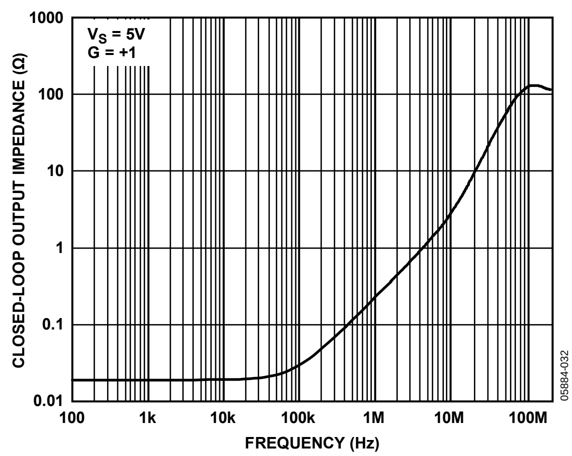


Figure 21. Output Impedance vs. Frequency Enabled

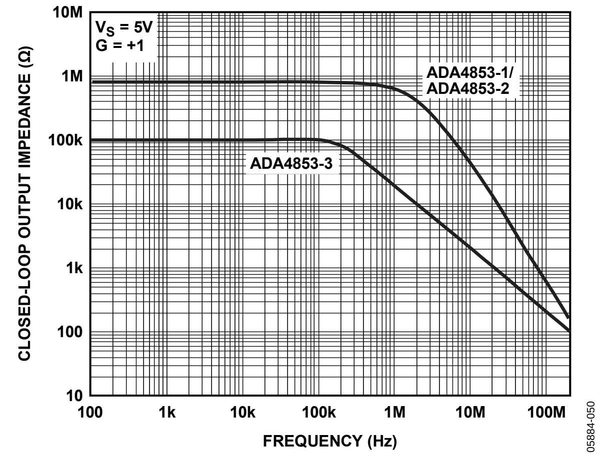


Figure 22. Output Impedance vs. Frequency Disabled

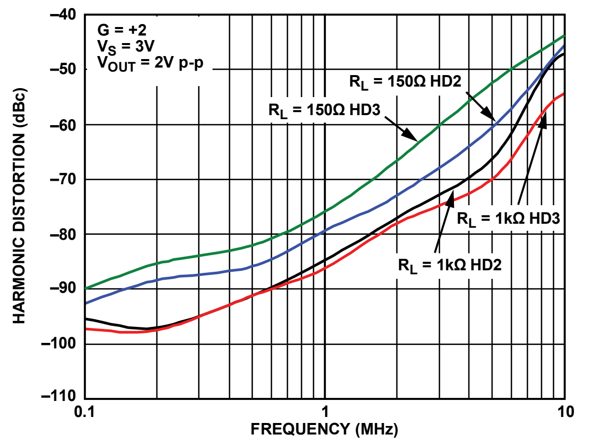


Figure 23. Harmonic Distortion vs. Frequency

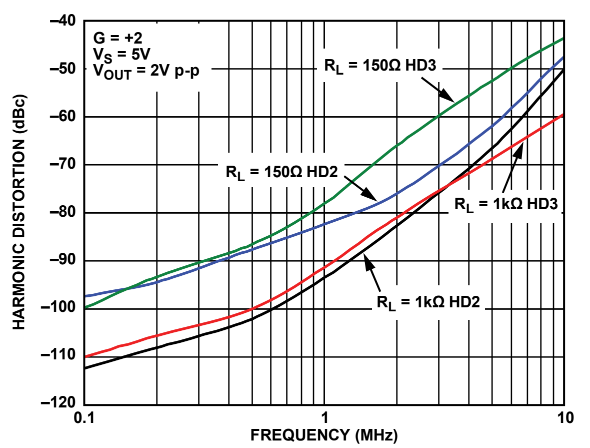


Figure 24. Harmonic Distortion vs. Frequency

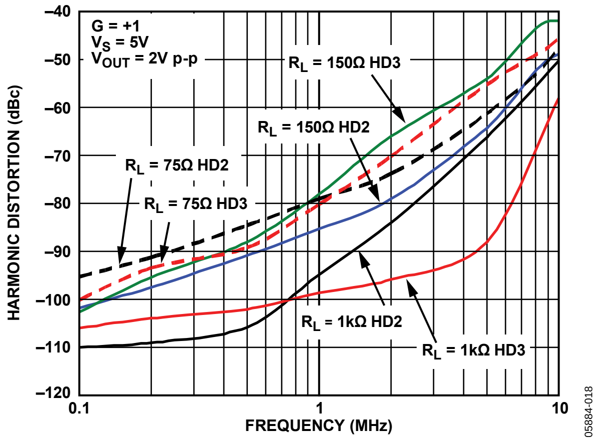


Figure 25. Harmonic Distortion vs. Frequency

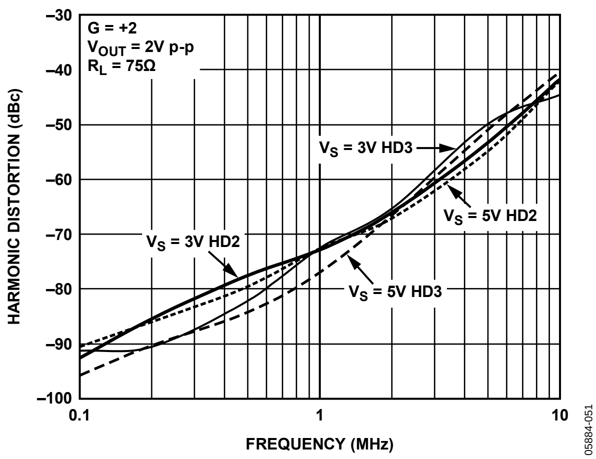


Figure 26. Harmonic Distortion vs. Frequency

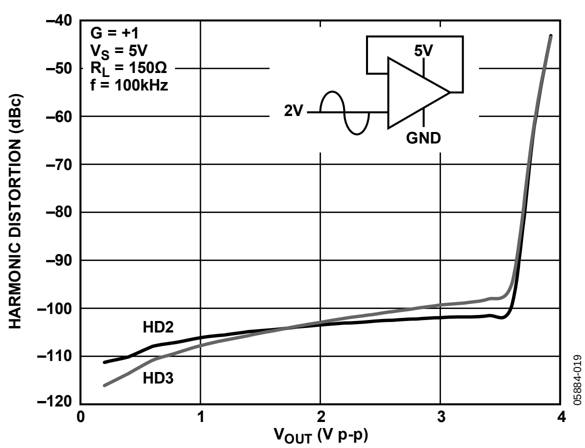


Figure 27. Harmonic Distortion for Various Output Voltages

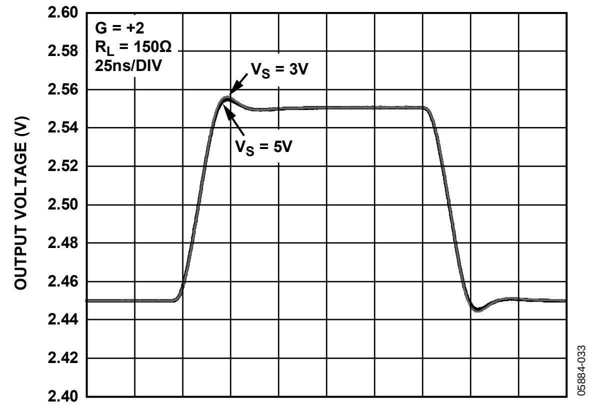


Figure 28. Small Signal Pulse Response for Various Supplies

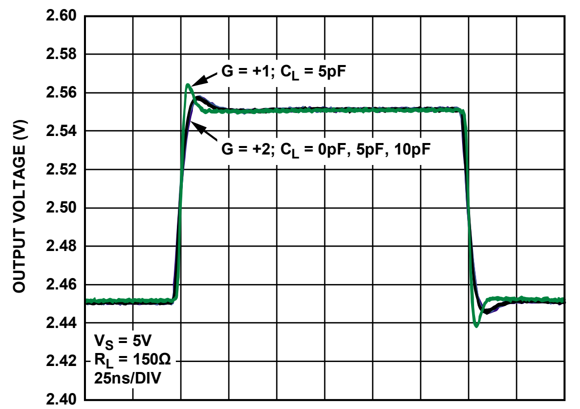


Figure 29. Small Signal Pulse Response for Various Capacitive Loads

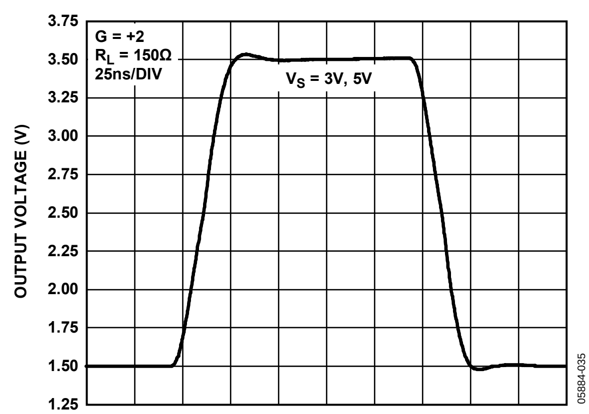


Figure 30. Large Signal Pulse Response for Various Supplies

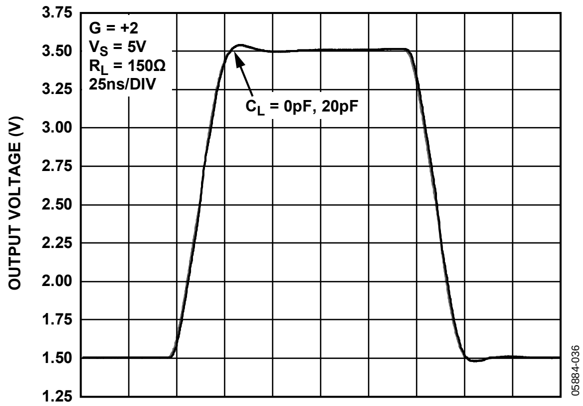


Figure 31. Large Signal Pulse Response for Various Capacitive Loads

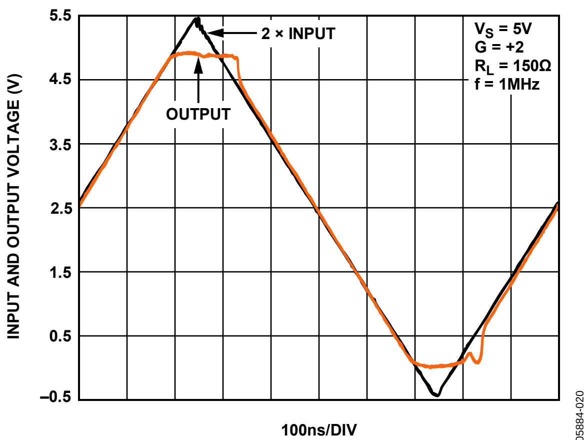


Figure 32. Output Overdrive Recovery

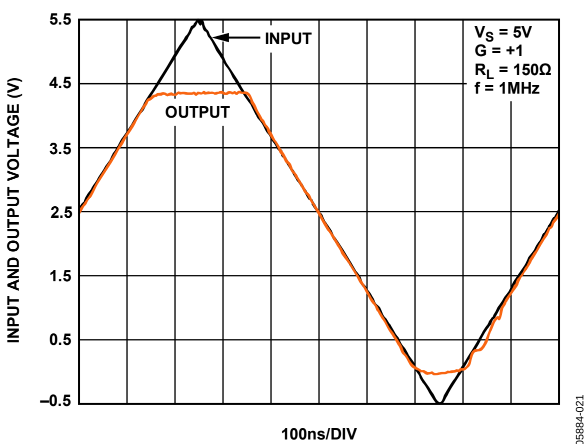


Figure 33. Input Overdrive Recovery

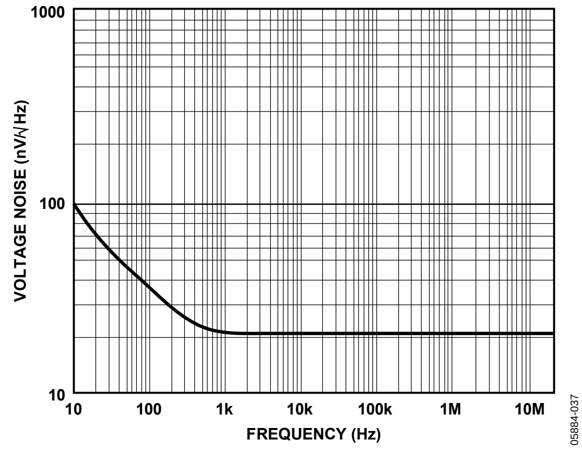


Figure 34. Voltage Noise vs. Frequency

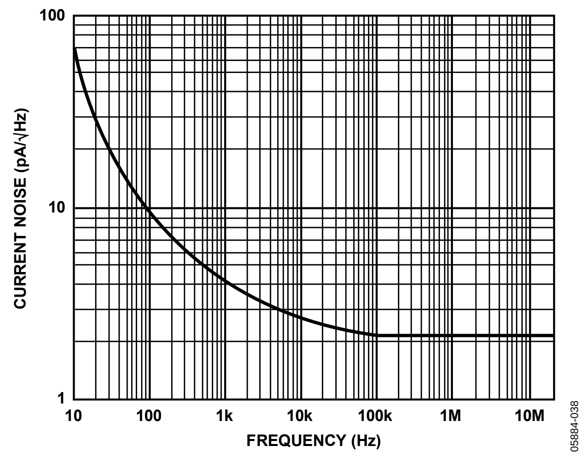


Figure 35. Current Noise vs. Frequency

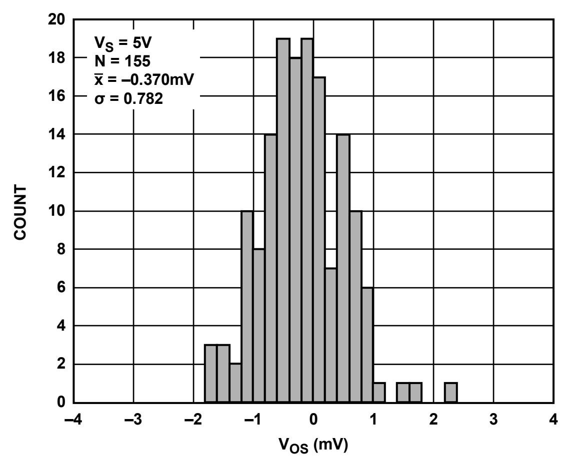


Figure 36. V_{OS} Distribution

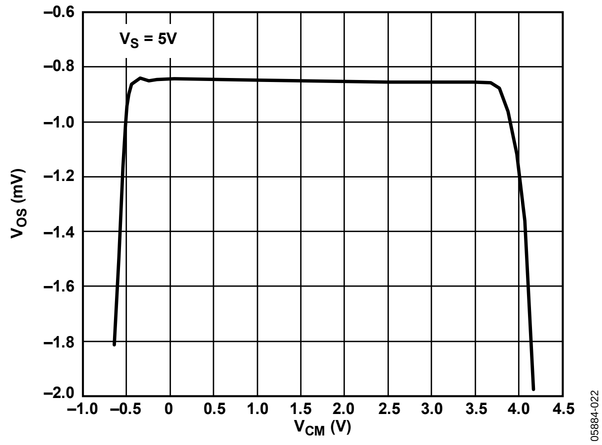


Figure 37. V_{OS} vs. Common-Mode Voltage

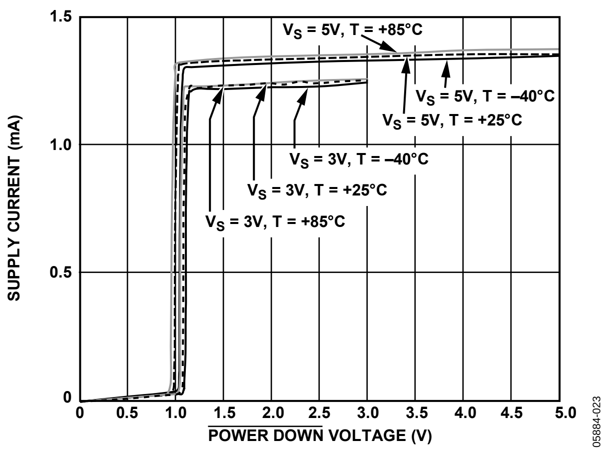


Figure 38. Supply Current vs. $\overline{\text{POWER DOWN}}$ Voltage

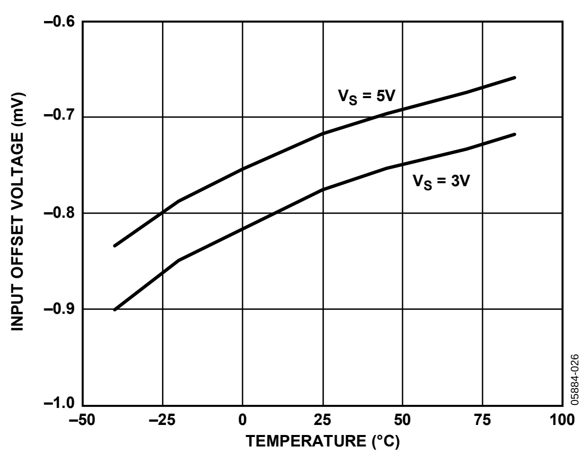


Figure 39. Input Offset Voltage vs. Temperature

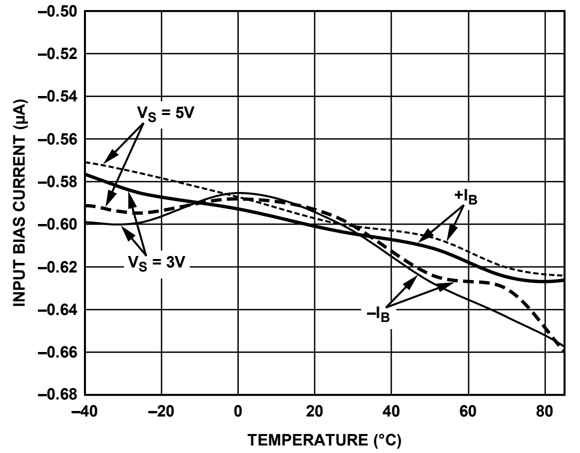


Figure 40. Input Bias Current vs. Temperature

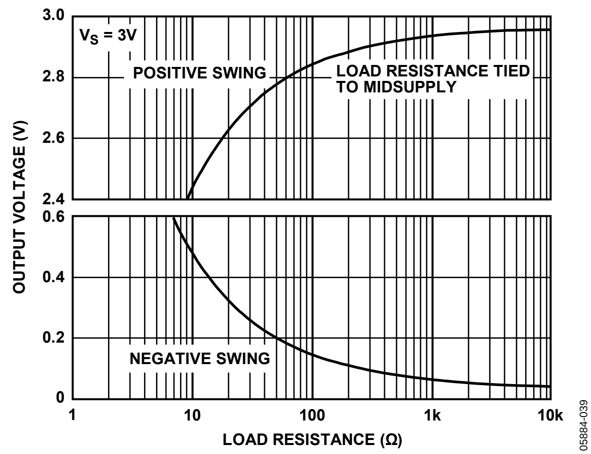


Figure 41. Output Voltage vs. Load Resistance

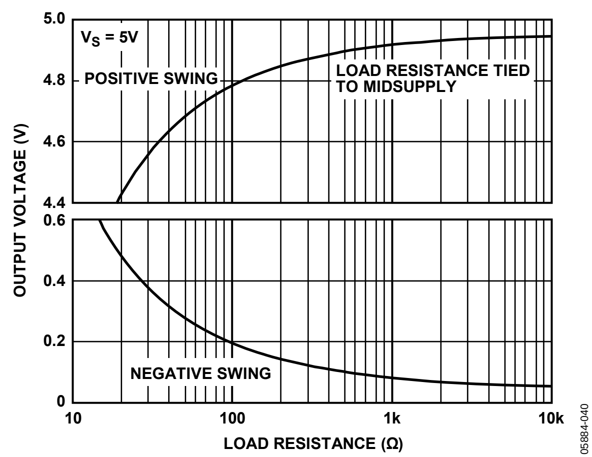


Figure 42. Output Voltage vs. Load Resistance

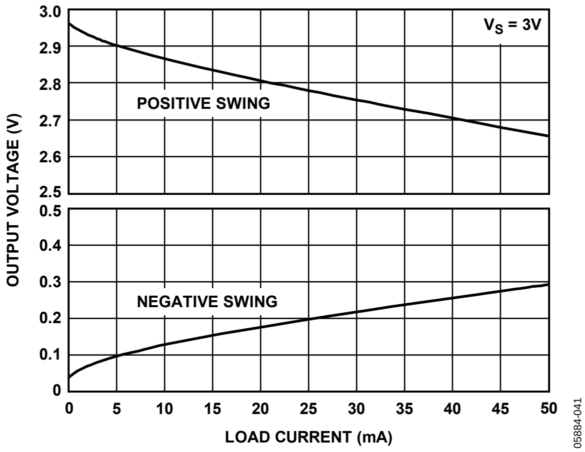


Figure 43. Output Voltage vs. Load Current

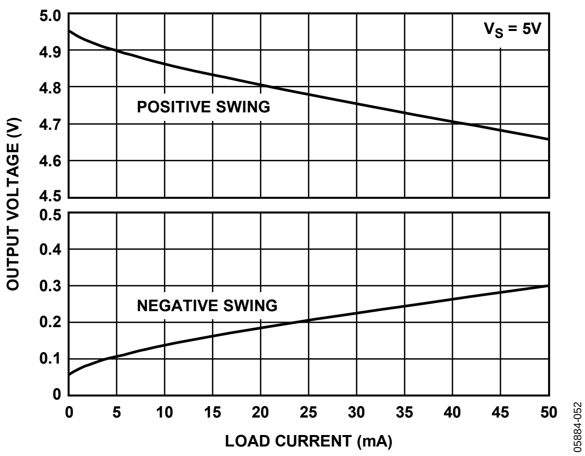


Figure 44. Output Voltage vs. Load Current

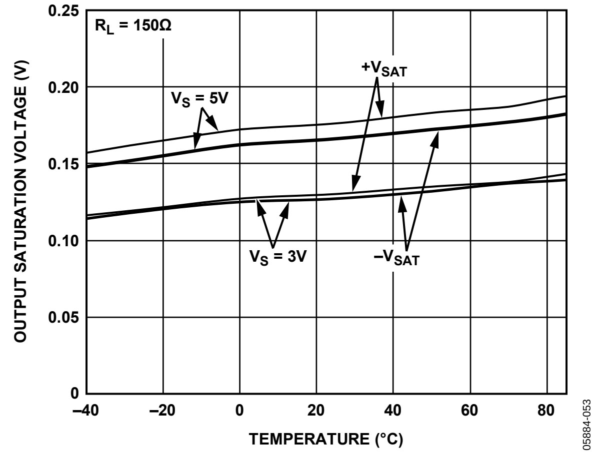


Figure 45. Output Saturation Voltage vs. Temperature for Various Supplies

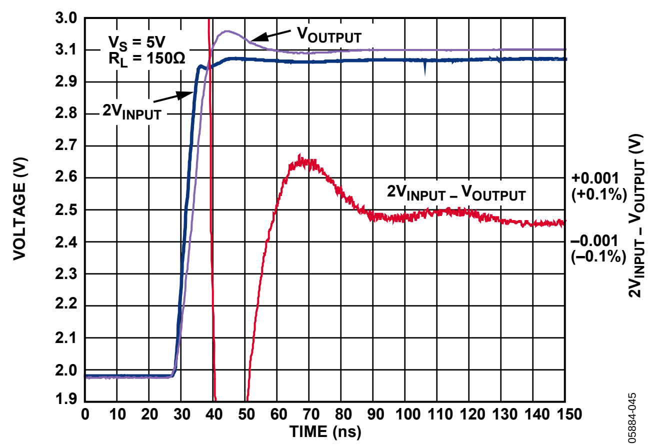


Figure 46. 0.1% Settling Time

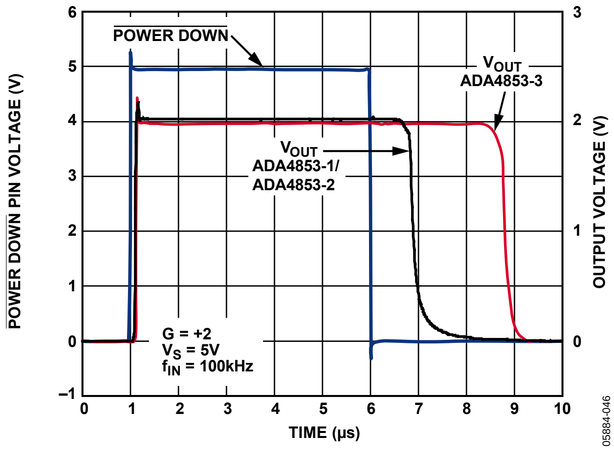


Figure 47. Enable/Disable Time

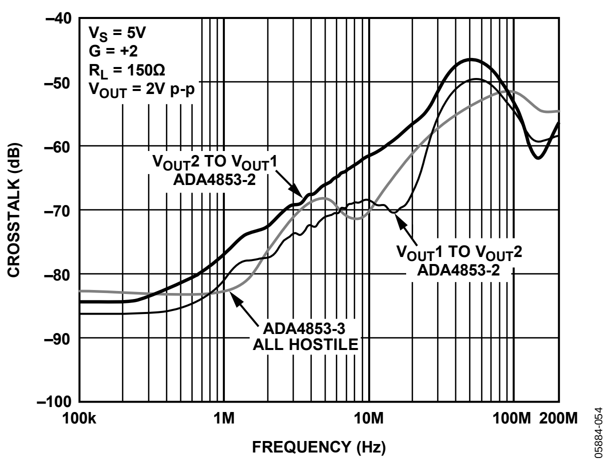


Figure 48. Crosstalk vs. Frequency

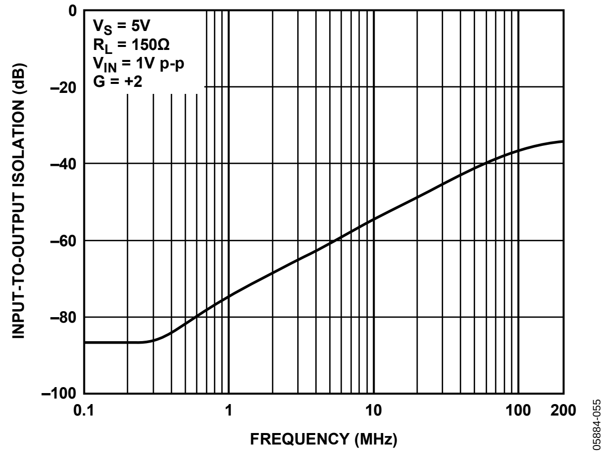


Figure 49. Input-to-Output Isolation, Chip Disabled

CIRCUIT DESCRIPTION

The ADA4853-1/ADA4853-2/ADA4853-3 feature a high slew rate input stage that is a true single-supply topology capable of sensing signals at or below the minus supply rail. The rail-to-rail output stage can pull within 100 mV of either supply rail when driving light loads and within 200 mV when driving 150 Ω. High speed performance is maintained at supply voltages as low as 2.65 V.

HEADROOM CONSIDERATIONS

The ADA4853-1/ADA4853-2/ADA4853-3 are designed for use in low voltage systems. To obtain optimum performance, it is useful to understand the behavior of the amplifiers as input and output signals approach their headroom limits. The amplifiers' input common-mode voltage range extends from the negative supply voltage (actually 200 mV below this) to within 1.2 V of the positive supply voltage.

Exceeding the headroom limits is not a concern for any inverting gain on any supply voltage, as long as the reference voltage at the amplifiers' positive input lies within the amplifiers' input common-mode range.

The input stage is the headroom limit for signals approaching the positive rail. Figure 50 shows a typical offset voltage vs. the input common-mode voltage for the ADA4853-1/ADA4853-2/ADA4853-3 on a 5 V supply. Accurate dc performance is maintained from approximately 200 mV below the negative supply to within 1.2 V of the positive supply. For high speed signals, however, there are other considerations. As the common-mode voltage gets within 1.2 V of positive supply, the amplifier responds well but the bandwidth begins to drop as the common-mode voltage approaches the positive supply. This can manifest itself in increased distortion or settling time. Higher frequency signals require more headroom than the lower frequencies to maintain distortion performance.

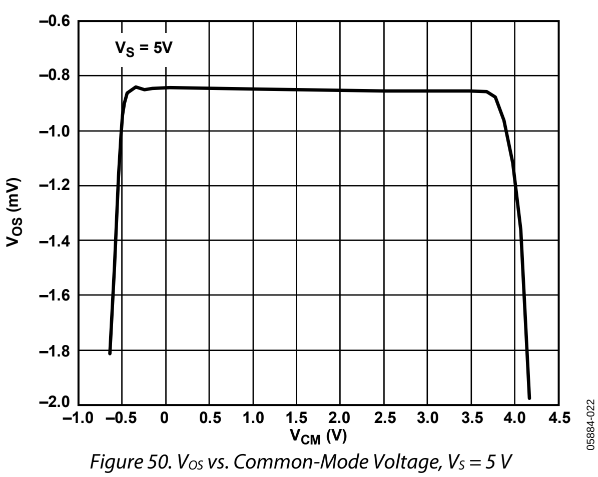


Figure 50. V_{OS} vs. Common-Mode Voltage, V_S = 5 V

For signals approaching the negative supply, inverting gain, and high positive gain configurations, the headroom limit is the output stage. The ADA4853-1/ADA4853-2/ADA4853-3 use a common-emitter output stage. This output stage maximizes the available output range, limited by the saturation voltage of the output transistors. The saturation voltage increases with the drive current that the output transistor is required to supply due to the output transistor's collector resistance.

As the saturation point of the output stage is approached, the output signal shows increasing amounts of compression and clipping. For the input headroom case, higher frequency signals require a bit more headroom than the lower frequency signals. Figure 27 illustrates this point by plotting the typical distortion vs. the output amplitude.

OVERLOAD BEHAVIOR AND RECOVERY

Input

The specified input common-mode voltage of the ADA4853-1/ADA4853-2/ADA4853-3 is 200 mV below the negative supply to within 1.2 V of the positive supply. Exceeding the top limit results in lower bandwidth and increased rise time. Pushing the input voltage of a unity-gain follower to less than 1.2 V from the positive supply leads to an increasing amount of output error as well as increased settling time. The recovery time from input voltages 1.2 V or closer to the positive supply is approximately 40 ns; this is limited by the settling artifacts caused by transistors in the input stage coming out of saturation.

The amplifiers do not exhibit phase reversal, even for input voltages beyond the voltage supply rails. Going more than 0.6 V beyond the power supplies turns on protection diodes at the input stage, greatly increasing the current draw of the devices.

APPLICATIONS INFORMATION

SINGLE-SUPPLY VIDEO AMPLIFIER

With low differential gain and phase errors and wide 0.5 dB flatness, the ADA4853-1/ADA4853-2/ADA4853-3 are ideal solutions for portable video applications. Figure 51 shows a typical video driver set for a noninverting gain of +2, where $R_F = R_G = 1\ k\Omega$. The video amplifier input is terminated into a shunt 75 Ω resistor. At the output, the amplifier has a series 75 Ω resistor for impedance matching to the video load.

When operating in low voltage, single-supply applications, the input signal is only limited by the input stage headroom.

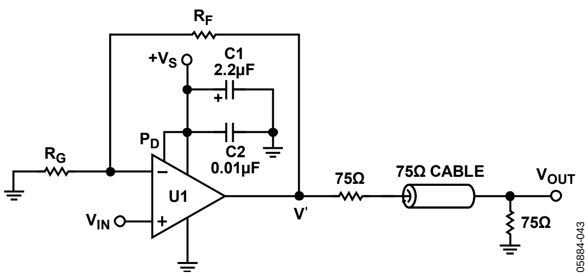


Figure 51. Video Amplifier

POWER SUPPLY BYPASSING

Attention must be paid to bypassing the power supply pins of the ADA4853-1/ADA4853-2/ADA4853-3. High quality capacitors with low equivalent series resistance (ESR), such as multilayer ceramic capacitors (MLCCs), should be used to minimize supply voltage ripple and power dissipation. A large, usually tantalum, 2.2 µF to 47 µF capacitor located in proximity to the ADA4853-1/ADA4853-2/ADA4853-3 is required to provide good decoupling for lower frequency signals. The actual value is determined by the circuit transient and frequency requirements. In addition, 0.1 µF MLCC decoupling capacitors should be located as close to each of the power supply pins as is physically possible, no more than ⅛ inch away. The ground returns should terminate immediately into the ground plane. Locating the bypass capacitor return close to the load return minimizes ground loops and improves performance.

LAYOUT

As is the case with all high speed applications, careful attention to printed circuit board (PCB) layout details prevents associated board parasitics from becoming problematic. The ADA4853-1/ADA4853-2/ADA4853-3 can operate at up to 100 MHz; therefore, proper RF design techniques must be employed. The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance return path. Removing the ground plane on all layers from the area near and under the input and output pins reduces stray capacitance. Signal lines connecting the feedback and gain resistors should be kept as short as possible to minimize the inductance and stray capacitance associated with these traces. Termination resistors and loads should be located as close as possible to their respective inputs and outputs. Input and output traces should be kept as far apart as possible to minimize coupling (crosstalk) through the board. Adherence to microstrip or stripline design techniques for long signal traces (greater than 1 inch) is recommended. For more information on high speed board layout, go to: www.analog.com to view *A Practical Guide to High-Speed Printed-Circuit-Board Layout*.

OUTLINE DIMENSIONS

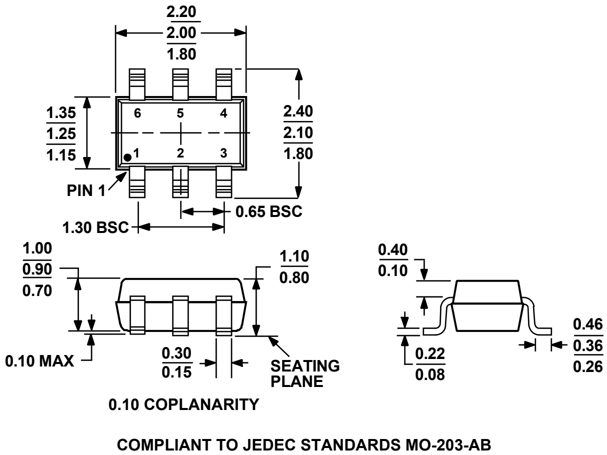


Figure 52. 6-Lead Thin Shrink Small Outline Transistor Package [SC70] (KS-6)—Dimensions shown in millimeters

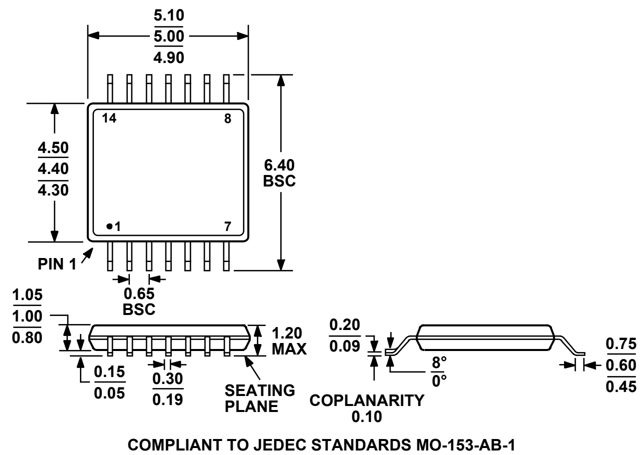


Figure 53. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)—Dimensions shown in millimeters

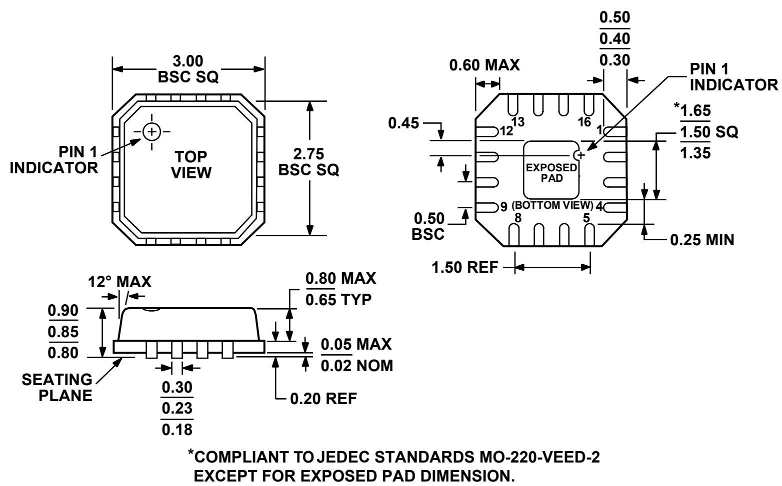


Figure 54. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ] 3 mm × 3 mm Body, Very Thin Quad (CP-16-3)—Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Ordering Quantity	Package Option	Branding
ADA4853-1AKSZ-R2[1]	−40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	250	KS-6	HEC
ADA4853-1AKSZ-R7[1]	−40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	3,000	KS-6	HEC
ADA4853-1AKSZ-RL[1]	−40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	10,000	KS-6	HEC
ADA4853-2YCPZ-R2[1]	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	250	CP-16-3	H0H
ADA4853-2YCPZ-RL[1]	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	5,000	CP-16-3	H0H
ADA4853-2YCPZ-RL7[1]	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	1,500	CP-16-3	H0H
ADA4853-3YCPZ-R2[1]	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	250	CP-16-3	H0L
ADA4853-3YCPZ-RL[1]	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	5,000	CP-16-3	H0L
ADA4853-3YCPZ-R7[1]	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	1,500	CP-16-3	H0L
ADA4853-3YRUZ[1]	−40°C to +105°C	14-Lead Thin Shrink Small Outline Package (TSSOP)	96	RU-14	
ADA4853-3YRUZ-RL[1]	−40°C to +105°C	14-Lead Thin Shrink Small Outline Package (TSSOP)	2,500	RU-14	
ADA4853-3YRUZ-R7[1]	−40°C to +105°C	14-Lead Thin Shrink Small Outline Package (TSSOP)	1,000	RU-14	

[1] Z = RoHS Compliant Part.

D05884-0-10/07(C)